Amendment to the Specification

[0019] In this configuration, M5 402 and resistor 404 isolate[[s]] the drain of M3 300 from pad 204 to substantially prevent any ESD current at pad 204 from directly flowing into the drain of M3 300. A size of M3 300 added to a size of M5 402 is substantially less than a size of M2 106, as shown by the example below. This is at least partially because PMOS devices are less susceptible to ESD, so they do not need a larger size to prevent damage. Also, M5 402 does not need to meet any operational specifications, so it can be only large enough to protect M3 300 from ESD.

[0020] FIG. 5 is a schematic diagram of system 200 according to an embodiment of the present invention. A main difference between FIGS. 4 and 5 is that ESD protection system 206" includes an NMOS transistor M6 500 with its gate coupled to a power supply (not shown), which replaces M5 402 in ESD protection system 206'. In this configuration, M6 500 and resistor 404 isolate[[s]] the drain of M3 300 from pad 204 to substantially prevent any ESD current at pad 204 from directly flowing into the drain of M3 300. A size of M3 300 added to a size of M5 500 is substantially less than a size of M2 106, as shown by the example below. This is because M6 500 does not need to meet any operational specifications, so it can be only large enough to protect itself and M3 300 from ESD.